Haneul Park

+1-217-721-0562 | skyp0714@gmail.com | skypark.me | skyp0714

Research Interests

Processor and subsystem (memory and network) architecture for datacenters

Education

- **University of Illinois, Urbana-Champaign** — *Aug 2023 - Current*
  Ph.D. candidate in Electrical and Computer Engineering — Champaign, IL
  - Advisor: Prof. Nam Sung Kim

- **Seoul National University** — *Mar 2018 - Aug 2023*
  B.S. in Electrical and Computer Engineering — Seoul, Korea
  - GPA: 4.17/4.3 (Summa Cum Laude)

Publications

C=Conference, S=Under Submission, J=Journal, M=Manuscript in progress

[S.1] **Haneul Park**, Grant Ayers, Nam Sung Kim, Philip Levis, and Brian Morris. **Rethinking Compression for CXL Memory Expanders at Hyperscale**. Under Submission to MICRO 2026.

[M.1] Kevin Zhou, **Haneul Park**, Ipoom Jeong, and Nam Sung Kim. **Mitigating I/O-Driven Contentions inside LLC with CXL-Memory-Aware Page Coloring**. Manuscript in progress.

[J.1] **Haneul Park**, Grant Ayers, Nam Sung Kim, Philip Levis, and Brian Morris. **Capacity–Latency Tradeoffs in CXL Memory Expanders at Hyperscale**. IEEE Computer Architecture Letters (CAL), July-December, 2026.

[C.1] **Haneul Park**, Siddharth Agarwal, Pradyun Narkadamilli, Kiung Jung, Yongjun Park, Ipoom Jeong, and Nam Sung Kim. **Compiler and System Optimizations for Gem5 Simulator**. IEEE International Symposium on Performance Analysis of System and Software (ISPASS), 2026 **[Best Paper Nomination]**

[C.2] **Haneul Park**, Jiaqi Lou, Sangjin Lee, Yifan Yuan, Kyoung Soo Park, Yongseok Son, Ipoom Jeong, and Nam Sung Kim. **A4: Microarchitecture-Aware LLC Management for Datacenter Servers with Emerging I/O Devices**. Proceedings of the 52nd Annual International Symposium on Computer Architecture (ISCA), 2025.

[C.3] Wenjing Jin, Wonsuk Jang, **Haneul Park**, Jongsung Lee, Soosung Kim, and Jae W. Lee. **DRAM Translation Layer: Software-Transparent DRAM Power Savings for Disaggregated Memory**. Proceedings of the 50th Annual International Symposium on Computer Architecture (ISCA), 2023.

Industry Experience

- **SK Hynix** — *June 2026 - Current*
  Global Internship at Solution Architecture — Bundang, Korea
  - Evaluating High Bandwidth Flash (HBF) in Attention/FFN disaggregated LLM serving systems.

- **Google** — *Jul 2024 - Dec 2025*
  Student researcher at Systems Research Group — Sunnyvale, CA
  - The first performance exploration of OCP CXL Tiered Memory Expander with inline compression that analyzes and quantifies latency-capacity tradeoffs at hyperscale.
  - Developed a novel synthetic benchmark for cold memory access patterns, tailored for evaluating tiered memory systems.

Research Experience

- **Research Assistant** — *Aug 2023 - Current*
  UIUC Future Architecture and System Technology for Scalable Computing — Champaign, IL
  - Advisor: Prof. Nam Sung Kim
  - Currently working on frontend optimizations for datacenter workloads, locality-aware TLP steering in intelligent PCIe switches, zero-copy/just-in-time DMA in CXL NICs, and PPA modeling of emerging memory cells for architectural simulation
  - Compiler and system optimizations for fast design-space exploration with gem5 simulator
  - Designing a fine-grain LLC partitioning scheme in CXL-enabled systems with emerging I/O devices
  - Designed *A4*, an LLC management framework for datacenter servers with emerging I/O devices
    - Discovered interference between I/O and CPU attributed to non-inclusive cache directory microarchitecture
    - Elucidated interference between high-speed I/O devices through Direct Cache Access (DCA)

- **Undergraduate Research Assistant** *Jul 2022 - Nov 2022*
  SNU Architecture and Code Optimization Lab Seoul, Korea
  ◦ Advisor: Prof. Jae W. Lee
  ◦ DRAM power saving for datacenters with an address translation layer in CXL-based memory pool
    – Rank-level power down by coalescing unallocated or cold memory regions
- **Undergraduate Research Assistant** *Jan 2022 - Jul 2022*
  SNU High Performance Computer System Lab Seoul, Korea
  ◦ Advisor: Prof. Jangwoo Kim
  ◦ Extended the Gem5 GPU simulator by enabling multi-GPU support for large-scale parallel systems
- **2022 Deep Learning Hardware Design Competition (AIX2022)** *Feb 2022 - Jul 2022*
  POLARIS; Korea Next-Generation Semiconductor Innovative Convergence University Seoul, Korea
  ◦ Designed and implemented a high-performance and power-efficient FPGA accelerator for CNN inference
  ◦ Oral presentation on IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2022

Honors and Awards

- **ISCA 25' Student Grant** | $400 *ISCA, USA, 2025*
- **2nd Place in 2022 Deep Learning Hardware Design Competition** | $2,000 *POLARIS, Korea, 2022*
- **OK Bae & Jung Scholarship** | $20,000 *OK Foundation, Korea, 2019*
- **Korea Presidential Science Scholarship** | one of 120 nationwide, $40,000 *Korea Student Aid Foundation, Korea, 2018*
- **Bronze Medalist in 2017 Korean Young Physicists' Tournament** *Korean Physical Society, Korea, 2017*
- **Korea Physics Olympiad (KPhO) National Team Selection Winter Camp** *Korean Physical Society (KPS), 2015/2016*

Areas & Skills

- **Area:** computer architecture, computer systems, microarchitecture, networking, performance engineering, HW-SW co-design, analytical and simulation-based performance modeling, FPGA, compiler, software engineering
- **Skill:** C/C++, Python, Verilog, Vivado HLS, Gem5, McPAT, Accel-sim, Linux, Lex/Yacc, Intel Pin, perf/Vtune, Pytorch, Pandas